Claims

[c1] What is claimed is:

1. A counter comprising:

a plurality of state units for generating a state, each state unit having a corresponding clock end for receiving a clock having a plurality of pulses; wherein each state unit is capable of updating the corresponding state when receiving different pulses from the clock according to a predetermined law while each of the state units receives the clock from the corresponding clock end; and a clock gating circuit electrically connected to the plurality of state units for selecting at least one first state unit and at least one second state unit from the plurality of state units according only to a fixed initial value and providing a triggering clock to the clock end of each first state unit and withholding the triggering clock from the clock end of each second state unit, such that second states corresponding to each second state unit are held constant while each of the first state units updates each state corresponding to the first state units according to different pulses of the triggering clock; the clock gating circuit not providing the triggering clock to each of the second state units according to each state changed of the first state unit, and not withholding the triggering clock from each of the first state units.

[c2] 2. The counter of claim 1 wherein the clock gating circuit selects corresponding different first state units and second state units from the plurality of state units while the initial value changes.

[c3] 3. The counter of claim 1 wherein each of the state units further comprises a setting end for receiving an initial state so that the state unit outputs the initial state while the state unit is triggered by a clock received from the corresponding clock end, then updates corresponding state output when receiving a following pulse of the clock according to the predetermined law.

[c4] 4. The counter of claim 3 wherein the counter is capable of setting each initial state of the state unit from each setting end of the state unit according to the initial value while the clock gating circuit selects the first state unit and the second state unit according to the initial value.

[c5] 5. The counter of claim 1 further comprising a lock circuit connected to the clock gating circuit for storing the initial value.

[c6] 6. The counter of claim 1 wherein each of the state units further comprises a flip-flop.

[c7] 7. A method for a counter, the counter comprising:
a plurality of state units for generating a state, each state unit having a corresponding clock end for receiving a clock having a plurality of pulses;
wherein each state unit is capable of updating the corresponding state when receiving different pulses from the clock according to a predetermined law while each of the state units receives the clock from the corresponding clock end; and
the method comprising:
selecting at least one first state unit and at least one second state unit from the plurality of state units according only to a fixed initial value and providing a triggering clock to the clock end of each first state unit and withholding the triggering clock from the clock end of each second state unit, such that second states corresponding to the second state unit are held constant while each of the first state units updates each state corresponding to the first state units according to different pulses of the triggering clock.

[c8] 8. The method of claim 7 further comprising selecting the first state unit and the second state unit according to the initial value but not providing the triggering clock to each of the second state units according to each state changed of the first state units, and not withholding the triggering clock from each of the first state units.

[c9] 9. The method of claim 7 further comprising selecting the first state unit and the second state unit according to the initial value for different initial values to select corresponding different first state units and second state units from the plurality of state units.

[c10] 10. The method of claim 7 wherein each of the state units further comprises a setting end for receiving an initial state so that the state unit outputs the initial state while the state unit is triggered by a clock received from the

corresponding clock end, then updates corresponding state output when receiving a following pulse of the clock according to the predetermined law.

[c11] 11. The method of claim 10 further comprising setting each initial state of the state unit from each setting end of the state unit according to the initial value while selecting the first state unit and the second state unit according to the initial value

12. The method of claim 7 wherein the counter further comprises a lock circuit connected to the clock gating circuit for storing the initial value.

[c12] 13. The method of claim 7 wherein each of the state units further comprises a flip-flop.